IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2823
Examiner: William D. Coleman
Confirmation No. 5545

In re PATENT APPLICATION of:

Applicant	: Shigayuki UEDA	)
Serial No.	: 09/665,663	)
Filed	: September 20, 2000	) **RESPONSE AFTER FINAL**
For	: SEMICONDUCTOR CHIP AND METHOD OF PRODUCING THE SAME	)
Attorney Ref.	: AI 281	)

BOX AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Final Examiner's Action mailed July 11, 2003, the due date of which has been extended by a Petition for a one-month Extension of Time filed herewith, to expire on November 12, 2003, 2003. The Action has been received and its contents carefully considered. Reconsideration of the application is requested.

Initially, the applicant wishes to note that the cited Japanese reference *Nakamura, Tomohito* (Japanese Patent Publication No. 2000-243904), hereinafter *Nakamura,* correspond to co-pending U.S. Patent Application Serial No. 09/511,104. The specification of *Nakamura*'s U.S. application substantially constitutes an English translation of the Japanese reference.

FEE ENCLOSED:$ 110.-
Please charge any further fee to our Deposit Account

The Examiner rejects claims 2-5, 7 and 10-14 under 35 U.S.C. 102(a) as being anticipated by *Nakamura, Tomohito* (Japanese Patent Publication No. 2000-243904), hereinafter *Nakamura.* The rejection respectfully is traversed.

Independent claims 11 and 12 are directed respectively to a semiconductor chip and a semiconductor device having a chip-on-chip structure. The structures of the chips are well explained in the applicant's Amendment dated May 15, 2003. In summary, with reference to the reference numbers in the drawings for purposes of explanation only, and with special attention to a particular commonly distinguishing feature of the claims, the chip (claim 11) or primary chip (claim 12) according to the invention includes a chip body 1 with internal wiring defining an external connection pad 15B and an internal connection pad 15A. A wire connecting portion 12, fabricated from a metal material having oxidation resistance, is electrically connected to the external connection pad 15B. An electrical contact projection BM fabricated from a metal having oxidation resistance, is electrically connected to the internal connection pad 15B. A surface protective film 16 covers the internal wiring and surface of the chip body 1 while contacting the wire connecting portion 12 and the projection BM, such that a segment of the wire connecting portion 12 and a segment of the projection BM project from the film 16. The projection BM is in the form of a bump and the wire connection portion 12 has a shape of the bump.

Nakamura fails to teach such a structure. For example, *Nakamura* does not teach (or even suggest) a wire connection portion fabricated from a metal material having oxidation resistance and electrically connected to an external connection pad, and a wire electrically connected to a segment of the wire connection portion.

According to the Action, the Examiner deems a pad 12 of *Nakamura* to correspond to a wire connection portion. There exists no such correspondence. The pad 12 of *Nakamura* is an ordinary pad that actually corresponds to the external connection pad BM of the present invention, and is not made of a metal material having oxidation resistance.

In greater detail, the Examiner refers to paragraph [0019] of the reference for an alleged teaching of "a wire connecting portion fabricated from a metal material 12 having oxidation resistance (gold, see paragraph [0019]) and electrically connected to the external connection pad BS/BM". The Examiner here misdescribes the pad 12 of *Nakamura*.

Firstly it is noted that the pad 12 of *Nakamura* is illustrated in Fig. 1 as projecting from a surface of a semiconductor chip 1, but this is for purposes of illustrating only parts of the overall structure. Missing in this figure is the insulation film 22 (which may correspond to the interlayer insulator 14 of the illustrated embodiment of the present invention) and the protective coat 24 (which may correspond to the surface protective film 16 of the illustrated embodiment of the present invention). Both are shown in the detail of Fig. 2 of *Nakamura* with respect to an area of the internal wiring 23 (which area corresponds to the internal connection pad 15A of the illustrated embodiment of the present invention). Thus, there is no disclosure that the pad 12 of *Nakamura* projects from the surface of a protective film (such as does the wire connection portion of the invention). Rather it would be covered in *Nakamura* by the protective coat 24 in a manner similar to its covering of the area of internal wiring 23 as shown in Fig. 2 of *Nakamura*.

Moreover, it is noted that paragraph [0019] of *Nakamura* relied upon by the Examiner is directed to the bumps BM/BS that are part of the inter-chip connection between the primary chip 1

and the secondary chip 2. No mention is made of the pad 12 for external connection. Therefore, these bumps BM/BS of paragraph [0019] of *Nakamura* are corresponding to the electrical contact projection BM of the illustrated embodiment of the present invention, not the wire connection portion thereof. Thus, the paragraph describes the construction and materials of the bumps of only the inter-chip connection.

In view of at least the above, it is believed clear that *Nakamura* neither discloses nor suggests the chip structure recited in claims 11 and 12. The rejection accordingly should be withdrawn both as to claims 11 and 12 and their respective sets of depending claims 2-5, 13, and 7, 10, 14.

Based on the above, it is submitted that the application is in condition for allowance and such Notice, with allowed claims 2-5, 7 and 10-14, earnestly is solicited. Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such a conference.

Respectfully submitted,

November 12, 2003
Date

Steven M. Rabin - Reg. No. 29,102
RABIN & BERDO, P.C.
Telephone: 202-371-8976
Telefax: 202-408-0924
CUSTOMER NO. 23995

SMR/